CHIPHOMER TECHNOLOGY (SHANGHAI) LIMITED

CP2113 Datasheet

Dual-Channel current-matching Boost LED Drivers

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Dual-Channel WLED Drivers For Smart Phone

Features

- 2.7V to 5.5V Input Voltage
- Integrated 1.5A/40V MOSFET
- 1.2MHz Switching Frequency
- Dual Current Sinks of up to 30mA Current Each
- 1% Typical Current Matching and Accuracy
- 37.5V OVP Threshold
- Adaptive Boost Output to WLED Voltages
- Very Low Voltage Headroom Control (90mV)
- Flexible Digital and PWM Brightness Control
- 1-Wire Control Interface
- PWM Dimming Control Interface
- Up to 100:1 PWM Dimming Ratio
- Up to 10-bit Dimming Resolution
- Up to 90% Efficiency
- Built-in Soft Start
- Over Voltage Protection
- Built-in WLED Open/Short Protection
- Thermal Shutdown
- Support 2.2uH Inductor Application
- 9 BALL 1.31 mm x 1.31 mm CSP Package

Applications

- Smart Phones
- PDAs, Handheld Computers
- GPS Receivers
- Backlight for Small and Media Form Factor LCD Display with Single-Cell Battery Input

Description

The CP2113 is a dual-channel WLED driver which provide highly integrated solutions for single-cell Li-ion battery powered smart phone backlight.The device has a built-in high efficiency boost regulator with integrated 1.5A/40V power MOSFET and support as low as 2.7V input voltage. With two high current-matching capability current sink regulators, the devices can drive up to 10s2p WLED diodes. The boost output can automatically adjust to the WLED forward voltage and allow very low voltage headroom control, thus to improve LED strings efficiency effectively.

The CP2113 supports both of the PWM dimming interface and 1-Wire pulse dimming interface and can realize 9-bit brightness code programming.

The CP2113 integrates built-in soft start, over voltage/current protection, and thermal shut down protections.

The device is available in a space-saving 1.31 mm x 1.31 mm CSP package.

Pin Assignment

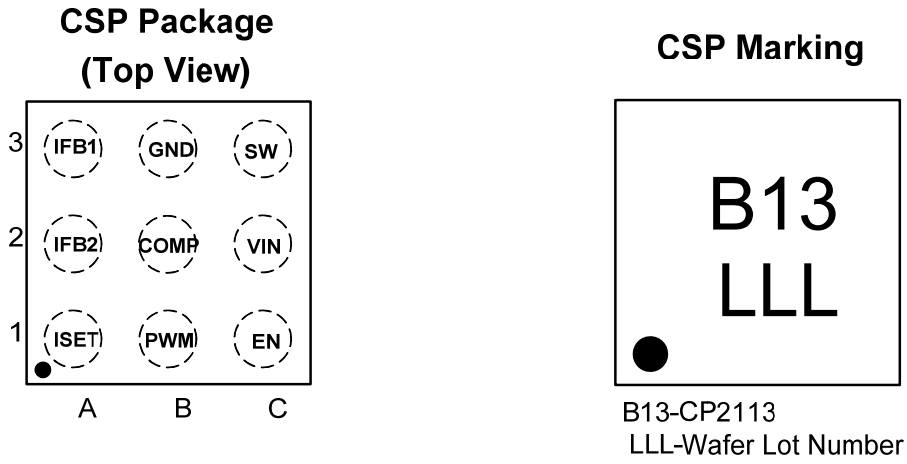


Figure 1 CP2113 Pin Assignment

Pin Definition

Pin	Name	Description
A1	ISET	Full-scale LED current set pin. Connecting a resistor to the pin programs the full-scale LED current
A2	IFB2	Regulated current sink input pin
A3	IFB1	Regulated current sink input pin
B1	PWM	PWM dimming signal input
B2	COMP	Output of the transconductance error amplifier. Connect external capacitor to this pin to compensate the boost loop
B3	GND	Ground
C1	EN	Enable control, and 1-Wire pulse signal input
C2	VIN	Supply input pin
C3	SW	Drain connection of the internal power MOSFET

Typical Application

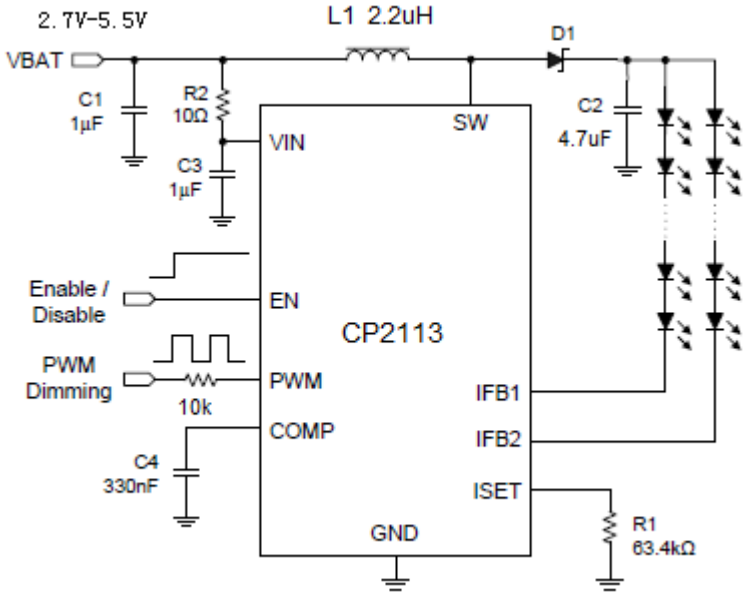
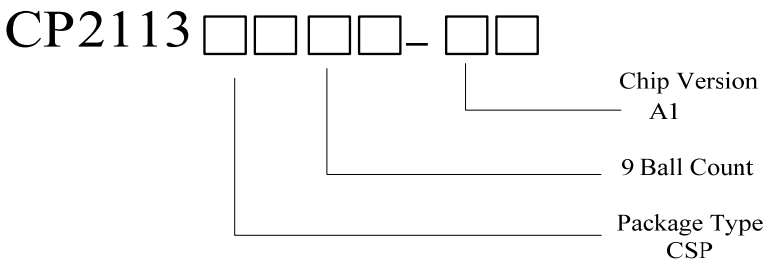


Figure 2 CP2113 Typical Application

Ordering Information

Order Number	Temperature Range	Package	RoHS	Marking	Shipping Type
CP2113CS9-A1	-40℃～85℃	CSP	Yes	B13 LLL	3000 Pcs/Reel

note：LLL refer to lot number



Absolute maximum ratings

Parameters	Value Range
VIN、EN、PWM、IFB1、IFB2	-0.3V～6V
COMP、ISET	-0.3～3V
SW	-0.3～40
Human Body Mode (100pF cap,1.5KΩ in series)	2000 V
Maximum Junction Temperature	150℃
Storage temperature range	-65℃~150℃
Operating temperature	-40℃～85℃
Junction-to-ambient thermal resistance θ_{JA}	107℃/W

Note：Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

Recommended Operating conditions

		Min	Typ	Max	Unit
V_{IN}	Input voltage range	2.7		5.5	V
V_{OUT}	Output voltage range	VIN		38	V
L	Inductor		2.2	10	uH
C_I	Input capacitor	1.0			uF
C_O	Output capacitor		4.7		uF
C_{COMP}	Compensation capacitor		330		nF
F_{PWM}	PWM dimming signal frequency	10		100	kHz
TA	Operating temperature	-40		85	℃
TJ	Operating junction temperature	-40		125	℃

Electrical Characteristics

V_{IN} = 3.6V, EN = high, PWM = high, IFB current = 20mA, T_J = -40°C to +125°C, typical values are at T_J = 25°C (unless otherwise noted)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
Power Supply						
VIN	Input voltage range		2.7		5.5	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} falling		2.2	2.3	V
		V_{IN} rising			2.45	

V_{VIN_HYS}	VIN UVLO hysteresis			100		mV
I_q	Operating quiescent current into VIN	Device enable, switching 1.2 MHz and no load, V_{IN} = 3.6V		1.2	2	mA
I_{SD}	Shutdown current	EN = low		1	2	uA
EN and PWM						
V_H	EN Logic high		1.2			V
V_L	EN Logic Low				0.4	V
V_H	PWM Logic high		1.2			V
V_L	PWM Logic Low				0.4	V
R_{PD}	EN pin and PWM pin internal pull-down resistor		400	800	1000	kΩ
t_{PWM_SD}	PWM logic low width to shutdown	PWM high to low	20			ms
t_{EN_SD}	EN logic low width to shutdown	EN high to low	2.5			ms
Current Regulation						
V_{ISET_full}	ISET pin voltage	Full brightness	1.204	1.229	1.253	V
K_{ISET_full}	Current multiplier	Full brightness		1030		
I_{FB_avg}	Current accuracy	I_{ISET} = 20 μA, D = 100%, 0°C to 70°C	-2%		2%	
		I_{ISET} = 20 μA, D = 100%, –40°C to 85°C	-2.3%		2.3%	
K_M	$(I_{MAX} – I_{AVG}) / I_{AVG}$	D = 100%		1%		
		D = 25%		1%		
I_{IFB_max}	Current sink max output current	I_{ISET} = 35 μA, each IFBx pin	30			mA
Power Switch						
$R_{DS(on)}$	Switch MOSFET on-resistance	V_{IN}=3.6V		0.25		Ω
		V_{IN}=3.0V		0.3		
I_{LEAK_SW}	Switch MOSFET leakage current	V_{SW} = 35 V, T_A = 25°C			1	uA
Oscillator						
f_{SW}	Oscillator frequency		1000	1200	1500	kHz
D_{max}	Maximum duty cycle	Measured on the drive signal of switch MOSFET	91	95		%
Boost voltage Control						
V_{IFB_reg}	IFBx feedback regulation voltage	IIFBx = 20mA, measured on IFBx pin which has a lower voltage		90		mV

I_{sink}	COMP pin sink current			12		uA
I_{source}	COMP pin source current			5		uA
G_{ea}	Error amplifier transconductance		30	55	80	Umho
R_{ea}	Error amplifier output resistance			45.5		MΩ
f_{ea}	Error amplifier crossover frequency	5pF connected to COMP pin		1.65		MHz
Protection						
I_{LIM}	Switch MOSFET current limit	D = D_{max}, 0°C to 70°C	1	1.5	2	A
I_{LIM_Start}	Switch MOSFET start up current limit	D = D_{max}		0.7		A
t_{Half_LIM}	Time window for half current limit			5		ms
V_{OVP_SW}	SW pin over voltage threshold		36	37.5	39	V
V_{OVP_IFB}	IFBx pin over voltage threshold	Measured on IFBx pin	4.2	4.5	4.8	V
1-Wire pulse Interface						
t_{es_delay}	1-Wire pulse detection delay	Measured from EN low to high	100			us
t_{es_det}	1-Wire pulse detection time	EN pin low time	260			us
t_{es_win}	1-Wire pulse detection window(1)	Measured from EN low to high	1			ms
t_{start}	Start time of program stream		2			us
t_{EOS}	End time of program stream		2		360	us
t_{H_LB}	High time of low bit (Logic 0)		2		180	us
t_{L_LB}	Low time of low bit (Logic 0)		2 x t_{H_LB}		360	us
t_{H_HB}	High time of high bit (Logic 1)		2 x t_{L_LB}		360	us
t_{L_HB}	Low time high bit (Logic 1)		2		180	us

$t_{valACKN}$	Acknowledge valid time				2	us
t_{ACKN}	Duration of acknowledge condition				512	us
V_{ACKNL}	Acknowledge output voltage low(2)	Open drain, R_{pullup} = 15 kΩ to VIN			0.4	V
Thermal Shutdown						
$T_{shutdown}$	Thermal shutdown threshold			160		℃
T_{hys}	Thermal shutdown hysteresis			15		℃

Note:

(1) To select 1-Wire pulse interface, after t_{es_delay} delay from EN low to high, drive EN pin to low for more than t_{es_det} before t_{es_win} expires.

(2) Acknowledge condition active 0, this condition is only applied when the RFA bit is set to 1. To use this feature, master must have an open drain output, and the data line needs to be pulled up by the master with a resistor load.

Block diagram

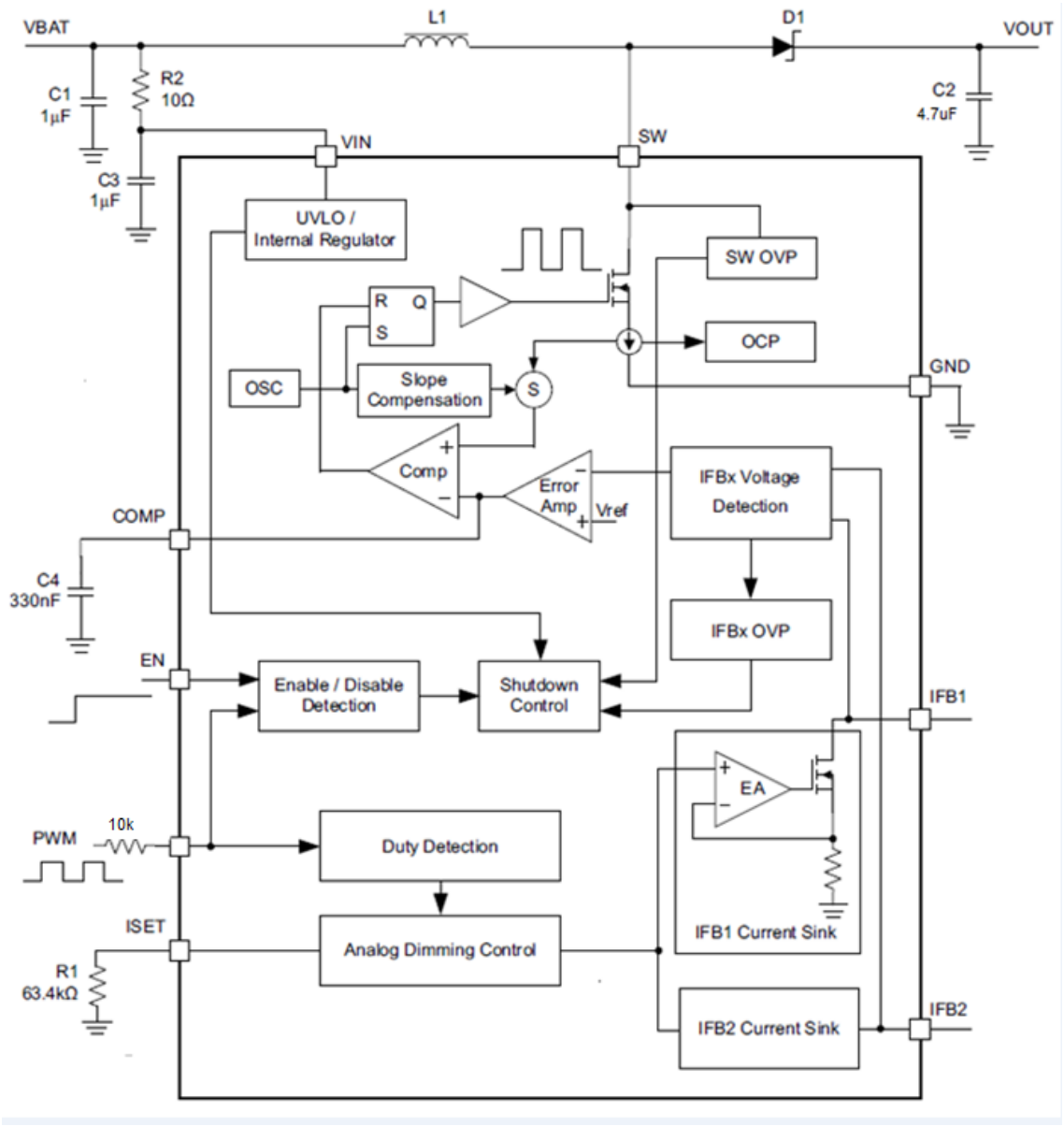


Figure 3 CP2113 Block Diagram

Operations

Normal operation

In order to provide high brightness backlighting for big size or high resolution smartphone panels, more and more white LED diodes are used. Having all LED diodes in a string improves overall current matching; however, the output voltage of a boost converter will be limited when input voltage is low, and normally the efficiency will drop when output voltage goes very high. Thus the LED diodes are arranged in two parallel strings.

The CP2113 is a high efficiency, dual-channel white LED driver for such smart phone backlighting applications. Two current sink regulators of high current-matching capability are integrated in the CP2113 to support dual LED strings connection and to improve the current balance and protect the LED diodes when either LED string is open or short.

CP2113 has integrated all of the key function blocks to power and control up to 20 white LED diodes. It includes a 40V/1.5A boost converter, two current sink regulators and protection circuit for over-current, over- voltage and thermal shutdown protection.

Boost Converter

The boost converter of the CP2113 integrates 40V 1.5A low side switch MOSFET and has a fixed switching frequency of 1.2MHz. The control architecture is based on traditional current-mode PWM control. For operation see the block diagram. Two current sinks regulate the dual-channel current and the boost output is automatically set by regulating IFBx pin's voltage. The output of error amplifier and the sensed current of switch MOSFET are applied to a control comparator to generate the boost switching duty cycle; slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%.

The forward voltages of two LED strings are normally different due to the LED diode forward voltage inconsistency, thus the IFB1 and IFB2 voltages are normally different. The CP2113 can select out the IFBx pin which has a lower voltage than the other and regulates its voltage to a very low value (90mV typical), which is enough for the two current sinks' headroom. In this way, the output voltage of the boost converter is automatically set and adaptive to LED strings' forward voltages, and the power dissipation of the current sink regulators can be reduced remarkably with this very low headroom voltage.

IFBx Pin Unused

If only one channel is needed, a user can easily disable the unused channel by connecting its IFBx pin to ground. If both IFBx pins are connected to ground, the IC will not start up.

Enable and Startup

In order to enable the IC from shutdown mode, three conditions have to be met: 1. POR (Power On Reset, that is, VIN voltage is higher than UVLO threshold), 2. Logic high on EN pin, 3. PWM signal (logic high or PWM pulses) on PWM pin. When these conditions are all met, an internal LDO linear regulator is enabled to provide supply to internal circuits and the IC can start up.

The CP2113 supports two dimming interfaces: 1-Wire pulse interface and PWM interface. CP2113 begins an 1-Wire pulse detection window after startup to detect which interface is selected. If the 1-Wire pulse interface is needed, signals of a specific pattern should be input into EN pin during the 1-Wire pulse detection window; otherwise, PWM dimming interface will be enabled (see details in 1-Wire pulse Interface).

After the 1-Wire pulse detection window, the CP2113 checks the status of IFBx pins. If one IFBx pin is detected to connect to ground, the corresponding channel will be disabled and removed from the control loop. Then the soft-start begins and the boost converter starts switching. If both IFBx pins are shorted to ground, the CP2113 will not start up.

Either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the device and the CP2113 enters into shutdown mode.

Softstart

Soft-start is implemented internally to prevent voltage over-shoot and in-rush current. After the IFBx pin status detection, the COMP pin voltage starts ramp up and the boost starts switching. During the beginning 5ms (t_{Half_LIM}) of the switching, the peak current of the switch MOSFET is limited at I_{LIM_Start} (0.7A typical) to avoid the input inrush current. After the 5ms, the current limit is changed to I_{LIM} (1.5A typical) to allow the normal operation of the boost converter.

Full-scale Current Program

The dual channels of the CP2113 can provide up to 30 mA current each. No matter either 1-Wire pulse interface or PWM interface is selected, the full-scale current (current when dimming duty cycle is 100%) of each channel should be programmed by an external resistor R_{ISET} at ISET pin according to Equation (1)

$$I_{FB\_full} = \frac{V_{ISET\_full}}{R_{ISET}} \times k_{ISET\_Full} \quad (1)$$

Where:

I_{FB_full}, full-scale current of each channel

K_{ISET_full} = 1030 (Current multiple when dimming duty cycle = 100%)

V_{ISET_full} = 1.229V (ISET pin voltage when dimming duty cycle = 100%)

R_{ISET} = ISET pin resistor

Brightness Control

The CP2113 controls the DC current of the dual channels to realize the brightness dimming. The DC current control is normally referred to as analog dimming mode. When the DC current of LED diode is reduced, the brightness is dimmed.

The CP2113 can receive either the PWM signals at the PWM pin (PWM interface) or digital commands at the EN pin (1-Wire pulse interface) for brightness dimming. If the 1-Wire pulse interface is selected, the PWM pin should be kept high; if PWM interface is selected, the EN pin should be kept high.

1-Wire pulse Interface

The EN pin features a simple digital interface to allow digital brightness control. The digital dimming interface can save the processor power and battery life as it does not require PWM signals all the time, and the processor can enter idle mode if possible. In order to enable the 1-Wire pulse interface, the following conditions must be satisfied and the specific digital pattern on the EN pin must be recognized by the IC every time the CP2113 starts up from shutdown mode.

1. VIN voltage is higher than UVLO threshold and PWM pin is pulled high.
2. Pull EN pin from low to high to enable the CP2113. At this moment, the 1-Wire pulse detection window starts.
3. After 1-Wire pulse detection delay time (t_{es_delay}, 100μs), drive EN to low for more than 1-Wire pulse detection time (t_{es_detect}, 260μs).

The third step must be finished before the 1-Wire pulse detection window (t_{es_win}, 1ms) expires, and once this step is finished, the 1-Wire pulse interface is enabled and the 1-Wire pulse communication can start. Refer to **Figure 4** for a graphical explanation.

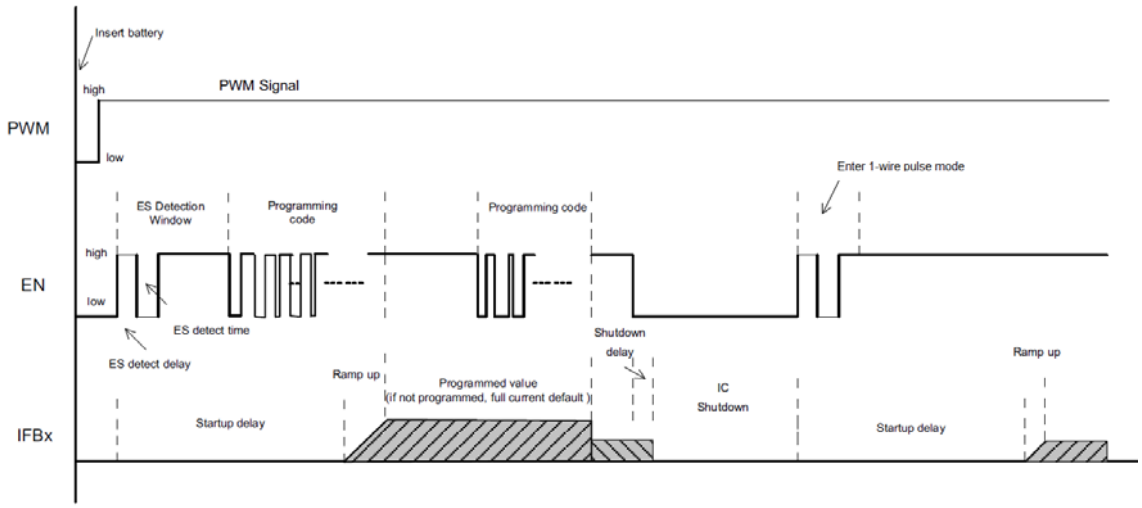


Figure 4 1-Wire Pulse Interface Detection

The CP2113 supports 9-bit brightness code programming. By the 1-Wire pulse interface, a master can program the 9-bit code D8(MSB) to D0(LSB) to any of 511 steps with a single command. The default code value of D8~D0 is “111111111” when the device is first enabled, and the programmed value will be stored in an internal register and set the dual-channel current according to Equation (2). The code will be reset to default value when the IC is shut down or disabled.

$$I_{FBx} = I_{FB\_full} \times \frac{Code}{511} \qquad (2)$$

Where

I_{FB_full}: the full-scale LED current set by the R_{ISET} at ISET pin

Code: the 9-bit brightness code D8~D0 programmed by 1-Wire pulse interface

When the 1-Wire pulse interface at EN pin is selected, the PWM pin can be connected to either VIN pin or a GPIO (refer to ADDITIONAL APPLICATION CIRCUITS). If PWM pin is connected to VIN pin, EN pin alone can enable and disable the IC: pulling EN pin low for more than 2.5ms disables the IC; if PWM pin is connected to a GPIO, both PWM and EN signals should be high to enable the IC, and either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms disables the IC.

1-Wire pulse Programming

1-Wire pulse is a simple but flexible one pin interface to configure the current of the dual channels. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor and the IC is the slave. Figure 5 and Figure 6 give an overview of the protocol used by CP2113. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. The device address byte D7(MSB)~D0(LSB) is fixed to 0x8F. The data byte includes 9 bits D8(MSB)~D0(LSB) for brightness information and an RFA bit. The RFA bit set to "1" indicates the Request for Acknowledge condition. The Acknowledge condition is only applied when the protocol is received correctly. The advantage of 1-Wire pulse compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

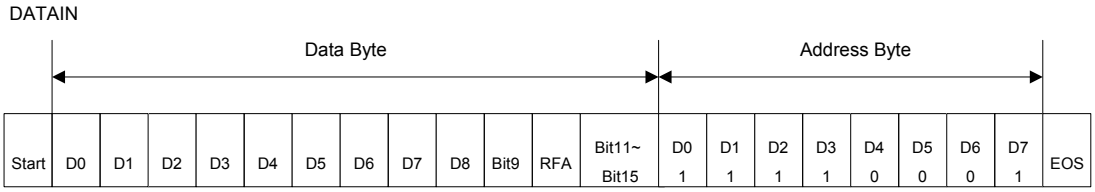


Figure 5 1-Wire Pulse Protocol Overview

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte (0x8F)	23 (MSB)	DA7	IN	DA7 = 1, MSB of device address
	22	DA6		DA6 = 0
	21	DA5		DA5 = 0
	20	DA4		DA4 = 0
	19	DA3		DA3 = 1
	18	DA2		DA2 = 1
	17	DA1		DA1 = 1
	16	DA0		DA0 = 1, LSB of device address
Data Byte	15	Bit 15	IN	No information. Write 0 to this bit.
	14	Bit 14		No information. Write 0 to this bit.
	13	Bit 13		No information. Write 0 to this bit.
	12	Bit 12		No information. Write 0 to this bit.
	11	Bit 11		No information. Write 0 to this bit.
	10	RFA		Request for acknowledge. If set to 1, IC will pull low the data line when it receives the command well. This feature can only be used when the master has an open drain output stage and the data line needs to be pulled high by the master with a pullup resistor; otherwise, acknowledge condition is not allowed and don't set this bit to 1.
	9	Bit 9		No information. Write 0 to this bit.
	8	D8		Data bit 8, MSB of brightness code
	7	D7		Data bit 7
	6	D6		Data bit 6
	5	D5		Data bit 5
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0, LSB of brightness code

Figure 6 1-Wire Pulse Bit Description

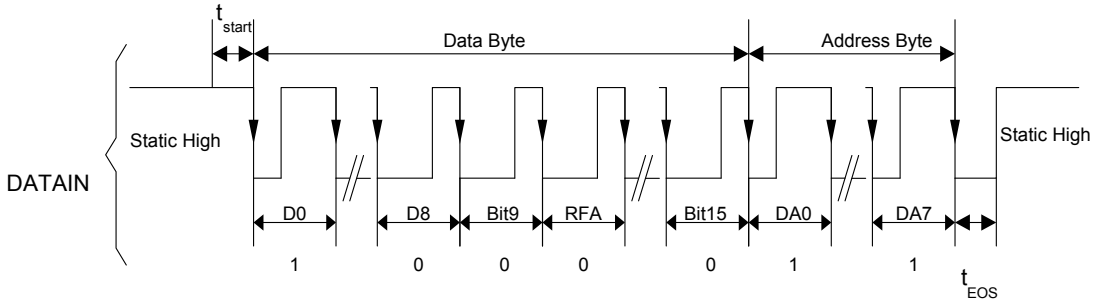


Figure 7 1-Wire Pulse Timing, with RFA=0

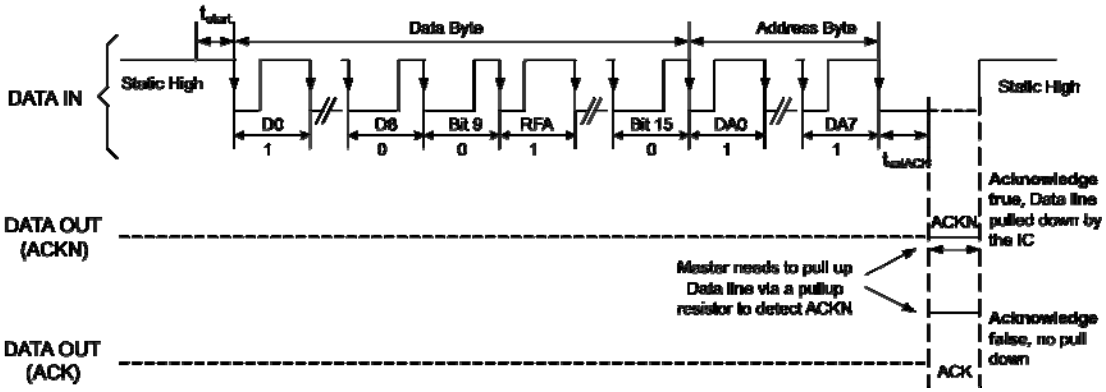


Figure 8 1-Wire Pulse Timing, with RFA=1

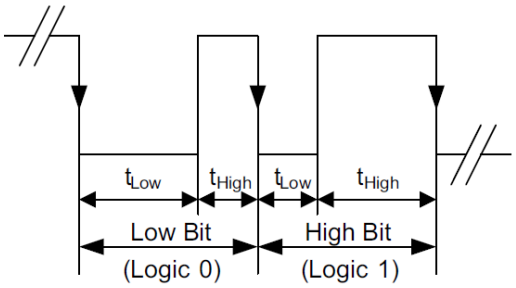


Figure 9 1-Wire Pulse — Bit Code

The 24-bit command should be transmitted with LSB first and MSB last. **Figure 7** shows the protocol without acknowledge request (Bit RFA = 0), **Figure 8** with acknowledge request (Bit RFA = 1). Before the command transmission, a start condition must be applied. For this, the EN pin must be pulled high for at least t_{start} (2μs) before the bit transmission starts with the falling edge. If the EN pin is already at high level, no start condition is needed. The transmission of each command is closed with an End of Stream condition for at least t_{EOS} (2μs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to **Figure 9**). It can be simplified to:

Low Bit(Logic 0)： $t_{LOW} \geq 2 \times t_{HIGH}$

High Bit(Logic 1)： $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1
- The transmitted device address matches with the device address of the IC
- Total 24 bits are received correctly

If above conditions are met, after t_{valACK} delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the EN pin low for the time t_{ACKN}, which is 512μs maximum, then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the IC has received the command correctly. The EN pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested when the master device has an open drain output. For a push-pull output stage, the use of a series resistor in the EN line to limit the current to 500μA is recommended to for such cases as:

- An accidentally requested acknowledge, or
- To protect the internal ACKN-MOSFET

PWM Control Interface

The PWM control interface is automatically enabled if the 1-Wire pulse interface fails to be enabled during startup. In this case, the CP2113 receives PWM dimming signals on the PWM pin to control the backlight brightness. When using PWM interface, the EN pin can be connected to VIN pin or a GPIO (refer to ADDITIONAL APPLICATION CIRCUITS). If EN pin is connected to VIN pin, PWM pin alone is used to enable and disable the IC: pulling PWM pin high or apply PWM signals at PWM pin to enable the IC and pulling PWM pin low for more than 20ms to disable the IC; if EN pin is connected to a GPIO, either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the IC. Only after both EN and PWM signals are applied, the CP2113 can start up. Refer to **Figure 10** for a graphical explanation.

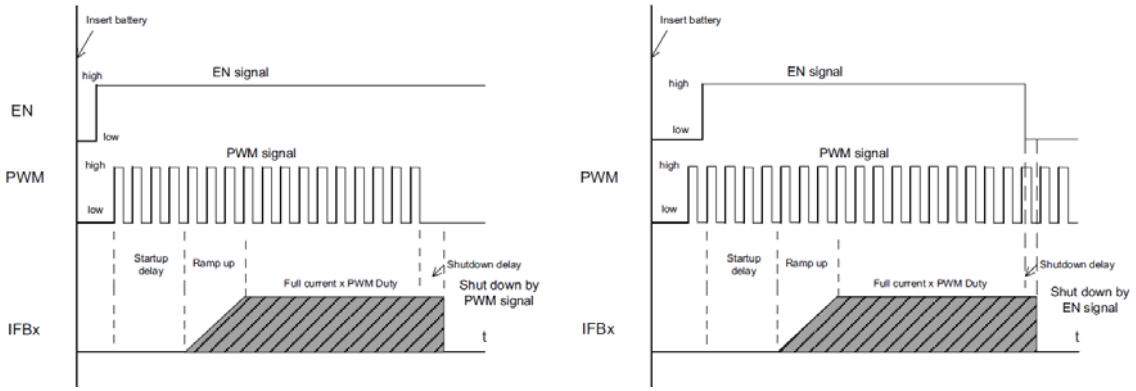


Figure 10 PWM Control Interface Detection

When the PWM pin is constantly high, the dual channel current is regulated to full-scale according to Equation (1). The PWM pin allows PWM signals to reduce this regulation current according to the PWM duty cycle; therefore, it achieves LED brightness dimming. The relationship between the PWM duty cycle and IFBx current is given by Equation (3)

$$I_{FBx} = I_{FB\_full} \times Duty \quad (3)$$

Where I_{FBx} is the current of each current sink, I_{FB_full} is the full-scale LED current, Duty is the duty cycle information detected from the PWM signals.

Undervoltage Lockout

An undervoltage lockout circuit prevents the operation of the device at input voltages below undervoltage threshold (2.2V typical). When the input voltage is below the threshold, the device is shutdown. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

Overvoltage Protection

Over voltage protection circuitry prevents IC damage as the result of white LED string disconnection or shortage. The CP2113 monitors the voltages at SW pin and IFBx pin during each switching cycle. No matter either SW OVP threshold V_{OVP_SW} or IFBx OVP threshold V_{OVP_FB} is reached due to the LED string open or short issue, the protection circuitry will be triggered. Refer to Figure 11 and Figure 12 for the protections.

If one LED string is open, its IFBx pin voltage drops, and the boost output voltage is increased by the control loop as it tries to regulate this lower IFBx voltage to the target value (90mV typical). For the normal string, its current is still under regulation but its IFBx voltage increases along with the output voltage. During the process, either the SW voltage reaches its OVP threshold V_{OVP_SW} or the normal string's IFBx pin voltage reaches the IFBx OVP threshold V_{OVP_FB}, then the protection circuitry will be triggered accordingly.

If both LED strings are open, both IFBx pins' voltages drop to ground, and the boost output voltage is increased by the control loop until reaching the SW OVP threshold V_{OVP_SW}, the SW OVP protection circuitry is triggered, and the IC is latched off. Only VIN POR or EN/PWM pin toggling can restart the IC.

One LED diode short in a string is allowed for the CP2113. If one LED diode in a string is short, the normal string's IFBx voltage is regulated to about 90mV, and the abnormal string's IFBx pin voltage will be higher. Normally with only one diode short, the higher IFBx pin voltage does not reach the IFBx OVP threshold V_{OVP_FB}, so the protection circuitry will not be triggered.

If more than one LED diodes are short in a string, as the boost loop regulates the normal string's IFBx voltage to 90mV, this abnormal string's IFBx pin voltage is much higher and will reach V_{OVP_FB}, then the protection circuitry is triggered.

The SW OVP protection will also be triggered when the forward voltage drop of an LED string exceeds the SW OVP threshold. In this case, the device turns off the switch FET and shuts down.

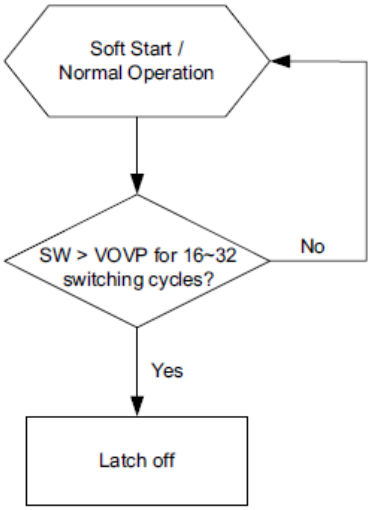


Figure 11 SW OVP Protection Action

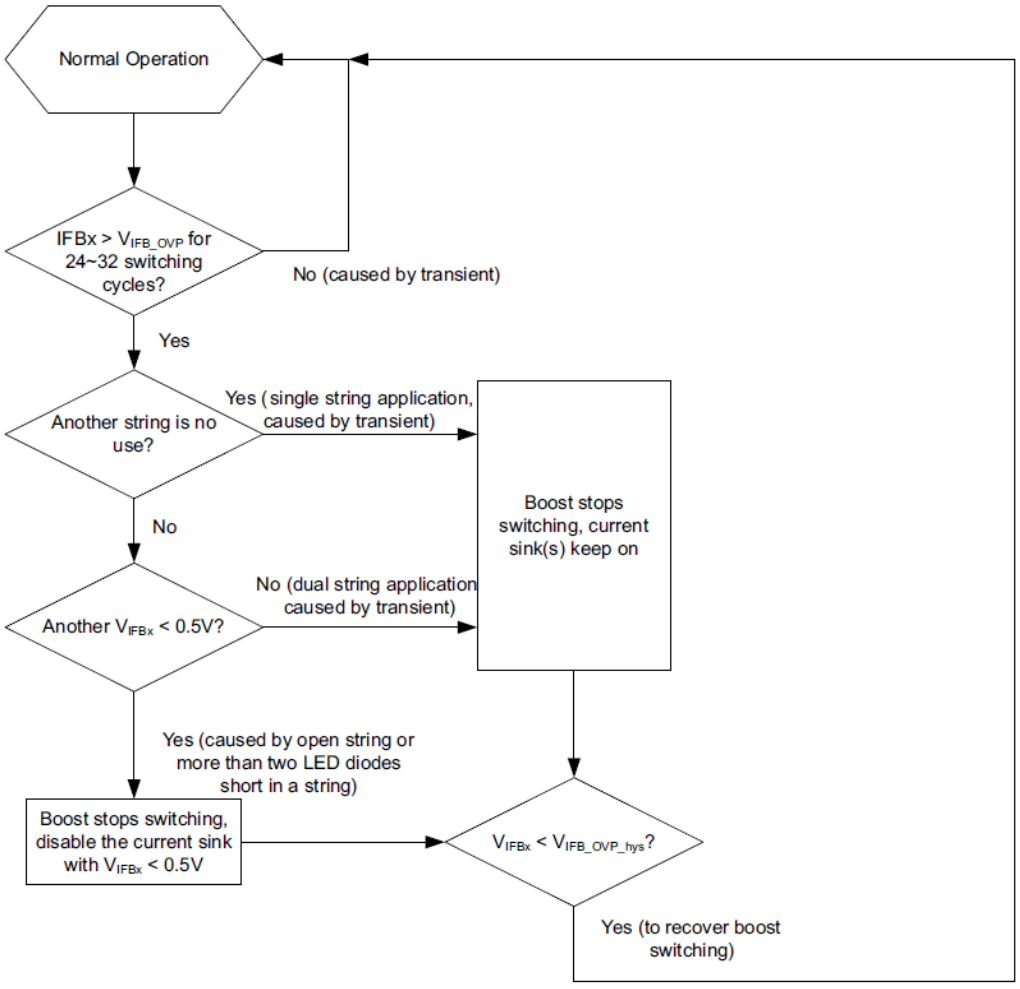


Figure 12 VIBx OVP Protection Action

Over Current Protection

The CP2113 has a pulse-by-pulse over-current limit. The boost switch turns off when the inductor current reaches this current threshold and it remains off until the beginning of the next switching cycle. This protects the CP2113 and external component under overload conditions.

Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

Application Information

Inductor selection

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The CP2113 is designed to work with inductor values from 2.2μH to 10μH to support all applications. A 2.2μH inductor is typically available in a smaller or lower profile package, while a 10μH inductor produces lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10μH inductor may maximize the controller's output current capability. A 22μH inductor can also be used for some applications, such as 6s2p and 7s2p, but may cause stability issue when more than eight WLED diodes are connected per string. Therefore, customers need to verify the inductor in their application if it is different from the values in RECOMMENDED OPERATING CONDITIONS.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation (4) to Equation (6) to calculate the inductor's peak current. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of the application. In order to leave enough design margin, the minimum switching frequency (1MHz for CP2113), the inductor value with –30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation.

In a boost regulator, the inductor DC current can be calculated as Equation (4)

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

Where

V_{OUT} = boost output voltage

I_{OUT} = boost output current

V_{IN} = boost input voltage

η = boost power conversion efficiency

The inductor current peak to peak ripple can be calculated as Equation (5)

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_S} \quad (5)$$

Where:

I_{PP} = inductor peak-to-peak ripple

L = inductor value

F_S = boost switching frequency

V_{OUT} = boost output voltage

V_{IN} = boost input voltage

Therefore, the peak current I_P seen by the inductor is calculated with Equation (6)

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (6)$$

Select an inductor with saturation current over the calculated peak current. If the calculated peak current is larger than the switch MOSFET current limit I_{LIM}, use a larger inductor, such as 10μH, and make sure its peak current is below I_{LIM}

Boost converter efficiency is dependent on the resistance of its current path, the switching losses associated with the switch MOSFET and power diode and the inductor's core loss. The CP2113 has optimized the internal switch resistance, however, the overall efficiency is affected a lot by the inductor's DC Resistance (DCR), Equivalent Series Resistance (ESR) at the switching frequency and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR/ESR conduction losses as well as higher core loss. Normally a datasheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, an inductor with lower DCR/ESR is recommended for CP2113 application. However, there is a trade off among inductor's inductance, DCR/ESR resistance, and its footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. **Figure 13** lists some recommended inductors for the CP2113. Verify whether the recommended inductor can support your target application by the calculations above as well as bench validation.

PART NUMBER	L (uH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	VENDOR
SWPA3015S2R2MT	2.2	78	1.6	Sunlord

Figure 13 Recommended Inductors

Schottky Diode Selection

The CP2113 demands a low forward voltage, high-speed and low capacitance Schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. Schottky diode 1N5819(1A/40V) is recommended for the CP2113.

Compensation Capacitor Selection

The compensation capacitor C4 (refer to ADDITIONAL APPLICATION CIRCUITS) connected from the COMP pin to GND, is used to stabilize the feedback loop of the CP2113. A 330nF ceramic capacitor for C4 is suitable for most applications. A 470nF is also OK for some

applications and customers are suggested to verify it in their applications.

Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. A 4.7μF capacitor is recommended for the loop stability consideration. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the output ripple can be calculated with Equation (7)

$$V_{ripple} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times C_{OUT}} \quad (7)$$

Where: V_{ripple} = peak-to-peak output ripple. The additional part of ripple caused by the ESR is calculated using $V_{ripple\_ESR} = I_{OUT} \times R_{ESR}$ and can be ignored for ceramic capacitors.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

Layout Consideration

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in ADDITIONAL APPLICATION CIRCUITS, needs to be close to the inductor, as well as the VIN pin and GND pin in order to reduce the input ripple seen by the IC. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R2 and C3 are recommended to filter and decouple the noise. In this case, C3 should be placed as close as possible to the VIN and GND pins. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and Schottky diode should be kept as short and wide as possible. The trace between Schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

Additional Application Circuits

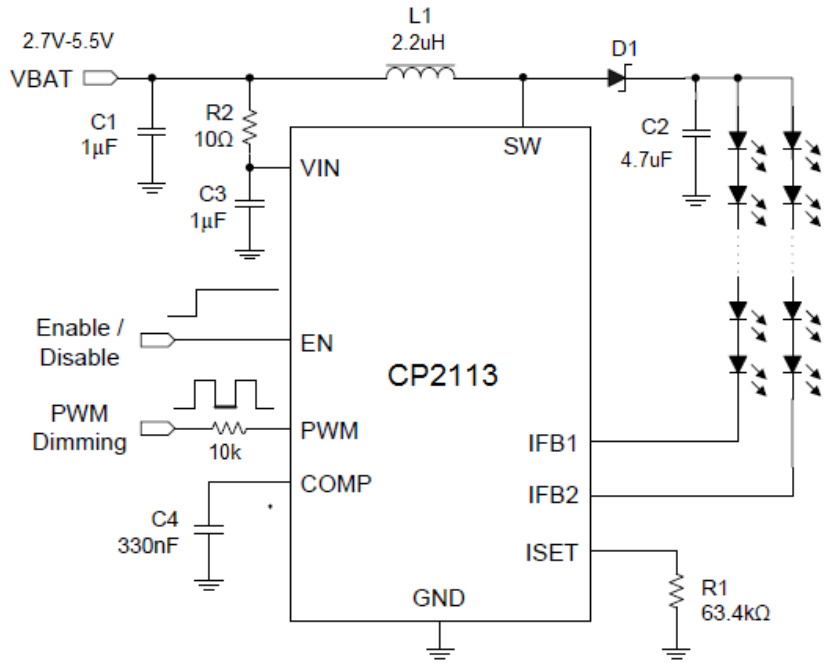


Figure 14 CP2113 Typical Application (PWM interface enabled, EN pin can be used to enable or disable the IC)

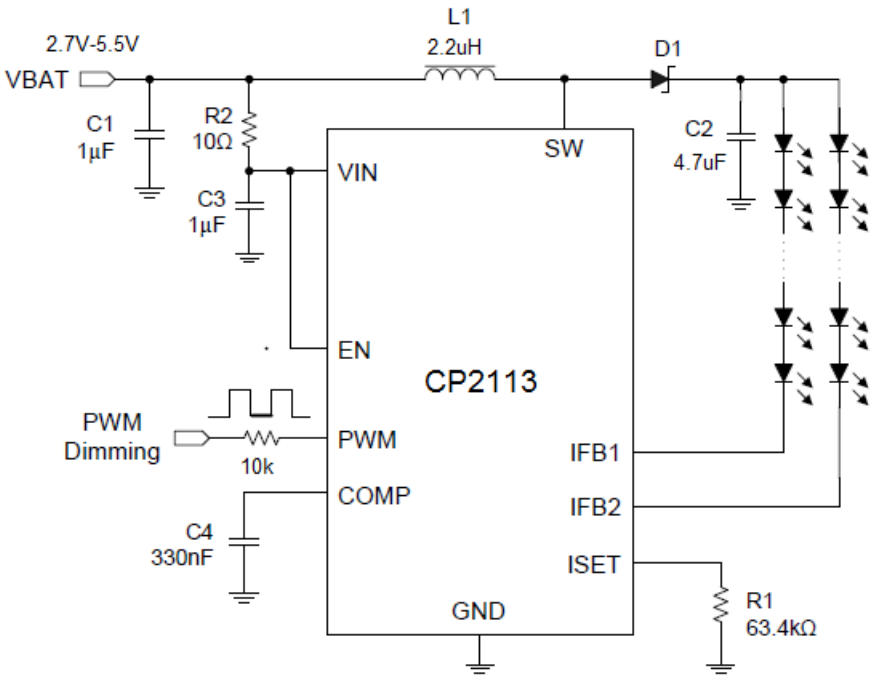


Figure 15 CP2113 Typical Application (PWM interface enabled, EN pin connected to VIN, only PWM signal is used to enable or disable the IC)

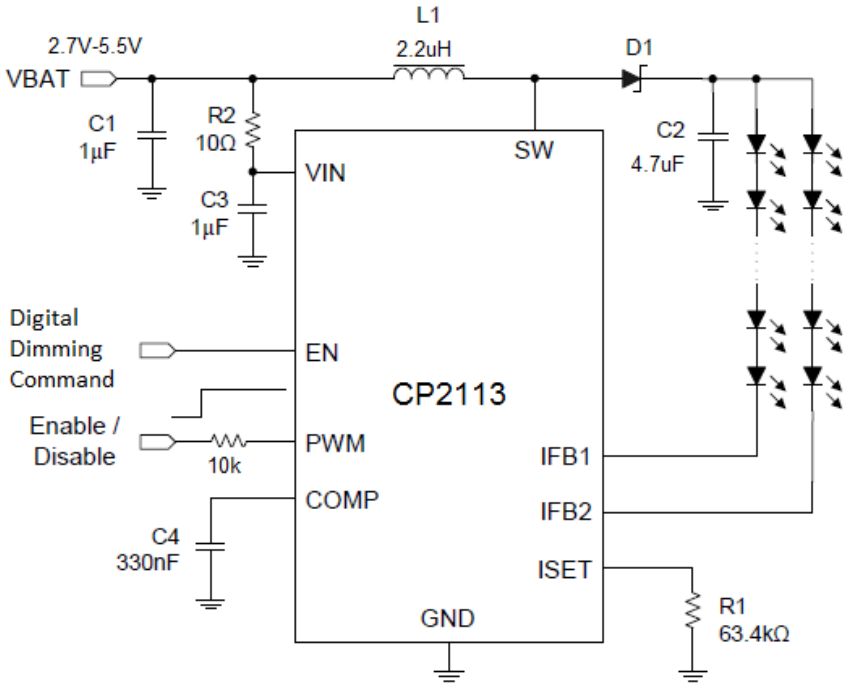


Figure 16 CP2113 Typical Application (1-wire pulse interface enabled, PWM pin can be used to enable or disable the IC)

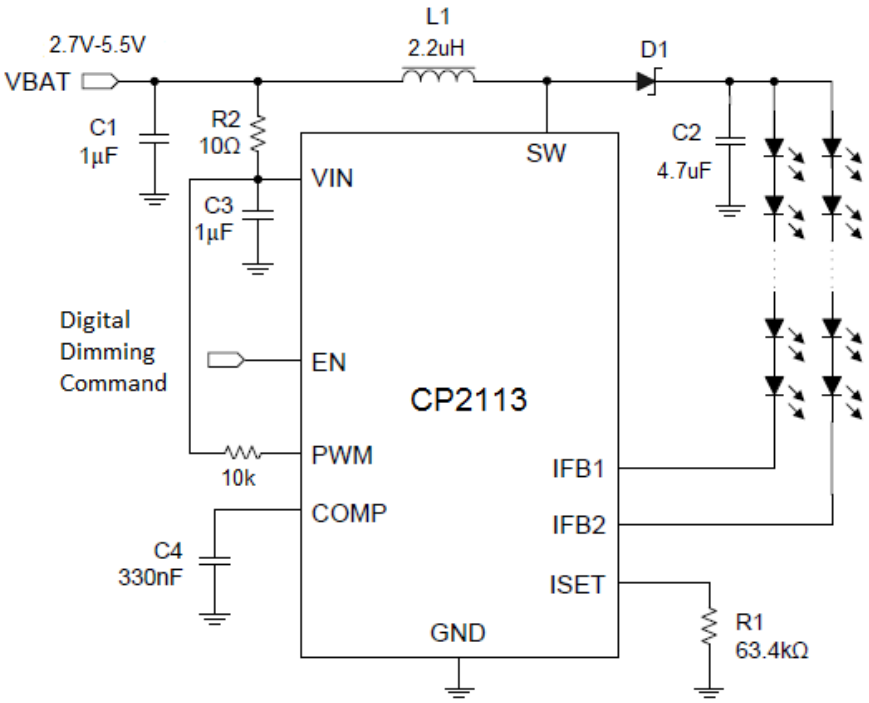


Figure 17 CP2113 Typical Application (1-wire pulse interface enabled, PWM pin connected to VIN, only EN signal is used to enable or disable the IC)

Typical Characteristics

(V_{IN} = 3.6V, L=2.2uH,unless otherwise noted)

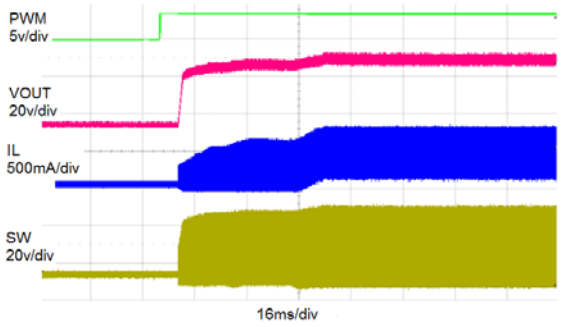


Figure 19 start up

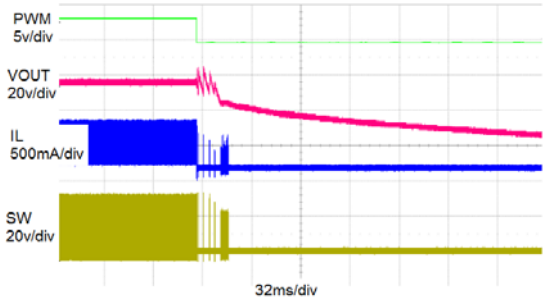


Figure 18 shut down

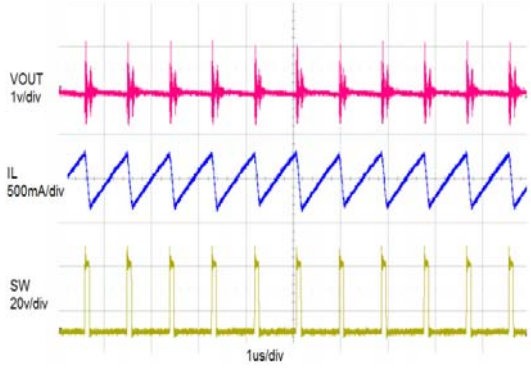


Figure 20 switching waveform, duty=100%

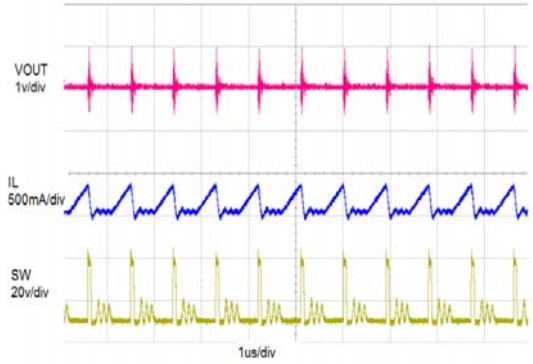


Figure 21 switching waveform, duty=20%

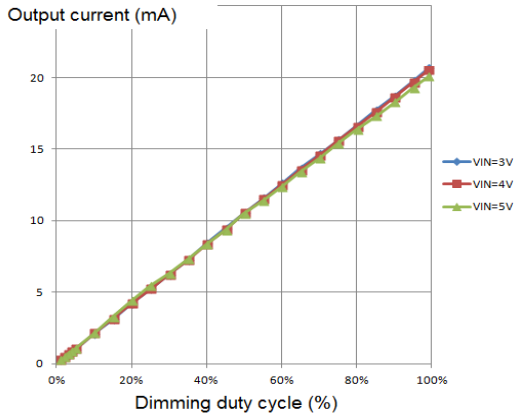


Figure 23 Dimming Linearity

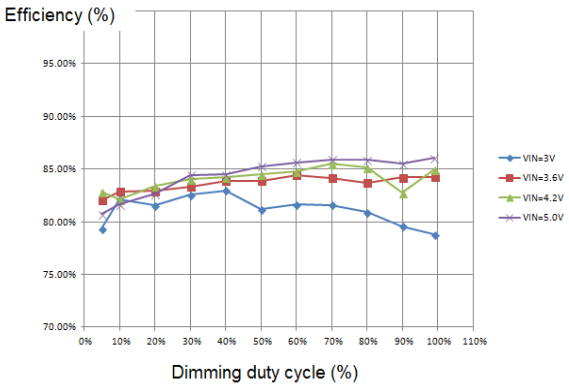
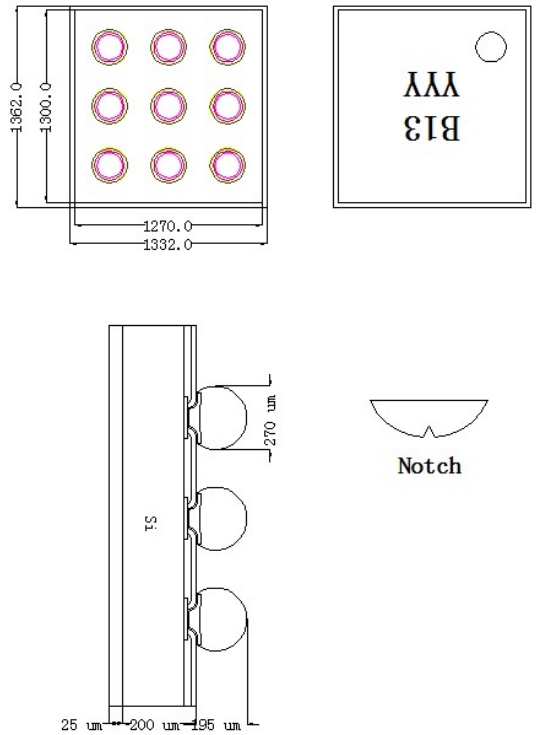


Figure 22 Efficiency, L=4.7uH

Package Information



Parameter	Nominal	Min	Max
	Millimeters		
Package Body Dimension X	1.302	1.272	1.332
Package Body Dimension Y	1.332	1.302	1.362
Package Height	0.42	0.39	0.45
Si thickness	0.2	0.1875	0.2125
Solder Bump Height	0.195	0.175	0.215
Solder Bump Diameter	0.27	0.25	0.29
Backside coating thickness	0.025	0.02	0.03
Total Ball Count per Die	9	/	/
Ball Pitch X axis	0.4	/	/
Ball Pitch Y axis	0.4	/	/

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